

Author index for papers in Volume 39

Pages are numbered consecutively through the volume: 1-280, January/March; 281-368, May; 369-520, July; 521-600, September; and 601-751, November.

- Acovic, A.**
229 see Shahidi, G. G.
- Adkisson, J. W.**
189 see Chesebro, D. G.
- Adkisson, J. W.**
215 see Koburger, C. W., III
- Adler, E., J. K. DeBrosse, S. F. Geissler, S. J. Holmes, M. D. Jaffe, J. B. Johnson, C. W. Koburger III, J. B. Lasky, B. Lloyd, G. L. Miles, J. S. Nakos, W. P. Noble, Jr., S. H. Voldman, M. Armacost, and R. Ferguson**
167 *The evolution of IBM CMOS DRAM technology*
- Adler, E.**
215 see Koburger, C. W., III
- Agarwal, R. C., S. M. Balle, F. G. Gustavson, M. Joshi, and P. Palkar**
575 *A three-dimensional approach to parallel matrix multiplication*
- Agnello, P. D.**
403 see Mann, R. W.
- Ainspan, H. A.**
63 see Kuchta, D. M.
- Ainspan, H. A.**
73 see Ewen, J. F.
- Anderson, C. J.**
229 see Shahidi, G. G.
- Armacost, M.**
167 see Adler, E.
- Avouris, Ph., I.-W. Lyo, and Y. Hasegawa**
603 *Probing electrical transport, electron interference, and quantum size effects at surfaces with STM/STS*
- Bakeman, P. E.**
215 see Koburger, C. W., III
- Balle, S. M.**
575 see Agarwal, R. C.
- Barrett, R. C.**
681 see Mamin, H. J.
- Barth, J. E., Jr.**
51 see Ellis, W. F.
- Bechade, R. A., and R. M. Houle**
93 *Digital delay line clock shapers and multipliers*
- Bergamaschi, R. A., R. A. O'Connor, L. Stok, M. Z. Moricz, S. Prakash, A. Kuehlmann, and D. S. Rao**
131 *High-level synthesis in an industrial environment*
- Bergendahl, A. S.**
215 see Koburger, C. W., III
- Bernstein, K., J. E. Bertsch, L. G. Heller, E. J. Nowak, and F. R. White**
33 *Reduced-voltage power/performance optimization of the 3.6-volt PowerPC 601 Microprocessor*
- Bertsch, J. E.**
33 see Bernstein, K.
- Bose, P., and S. Surya**
113 *Architectural timing verification of CMOS RISC processors*
- Botula, A. B.**
215 see Koburger, C. W., III
- Bouldin, D. P.**
465 see Hu, C.-K.
- Buchanan, D. A.**
245 see Taur, Y.
- Canora, F. J.**
63 see Kuchta, D. M.
- Chambliss, D. D., R. J. Wilson, and S. Chiang**
639 *The use of STM to study metal film epitaxy*
- Chang, W.**
215 see Koburger, C. W., III
- Chappell, B. A.**
229 see Shahidi, G. G.
- Chappell, T. I.**
229 see Shahidi, G. G.
- Chesebro, D. G., J. W. Adkisson, L. R. Clark, S. N. Eslinger, M. A. Faucher, S. J. Holmes, R. P. Mallette, E. J. Nowak, E. W. Sengle, S. H. Voldman, and T. W. Weeks**
189 *Overview of gate linewidth control in the manufacture of CMOS logic chips*
- Chiang, S.**
639 see Chambliss, D. D.

- Chu, J. O.**
629 see Lutz, M. A.
- Clark, L. R.**
189 see Chesebro, D. G.
- Clark, W. F.**
215 see Koburger, C. W., III
- Clevenger, L. A.**
403 see Mann, R. W.
- Colgan, E. G.**
419 see Licata, T. J.
- Comfort, J.**
229 see Shahidi, G. G.
- Cote, D. R., S. V. Nguyen, W. J. Cote, S. L. Pennington, A. K. Stamper, and D. V. Podlesnik**
437 *Low-temperature chemical vapor deposition processes and dielectrics for microelectronic circuit manufacturing at IBM*
- Cote, W. J.**
437 see Cote, D. R.
- Davari, B.**
215 see Koburger, C. W., III
- Davari, B.**
229 see Shahidi, G. G.
- DeBrosse, J. K.**
167 see Adler, E.
- Delgado-Frias, J. G.**
315 see Park, J.
- Dennard, R. H.**
229 see Shahidi, G. G.
- Dennard, R. H.**
547 see Deutsch, A.
- Deutsch, A., G. V. Kopcsay, C. W. Surovic, B. J. Rubin, L. M. Terman, R. P. Dunne, Jr., T. A. Gallo, and R. H. Dennard**
547 *Modeling and characterization of long on-chip interconnections for high-performance microprocessors*
- Dhong, S. H., M. Tanaka, S. W. Tomashot, and T. Kirihata**
105 *A low-noise TTL-compatible CMOS off-chip driver circuit*
- Dhong, S. H.**
43 see Sunaga, T.
- Divakaruni, S.**
51 see Ellis, W. F.
- Dreibelbis, J. H.**
51 see Ellis, W. F.
- Dunne, R. P., Jr.**
547 see Deutsch, A.
- Edelstein, D. C., G. A. Sai-Halasz, and Y.-J. Mii**
383 *VLSI on-chip interconnection performance simulations and measurements*
- Ellis, W. F., J. E. Barth, Jr., S. Divakaruni, J. H. Dreibelbis, A. Furman, E. L. Hedberg, H. S. Lee, T. M. Maffitt, C. P. Miller, C. H. Stapper, and H. L. Kalter**
51 *Multipurpose DRAM architecture for optimal power, performance, and product flexibility*
- Eslinger, S. N.**
189 see Chesebro, D. G.
- Ewen, J. F., M. Soyuer, A. X. Widmer, K. R. Wrenner, B. D. Parker, and H. A. Ainspan**
73 *CMOS circuits for Gb/s serial data communication*
- Fan, L. S.**
681 see Mamin, H. J.
- Faucher, M. A.**
189 see Chesebro, D. G.
- Feenstra, R. M.**
629 see Lutz, M. A.
- Ferguson, R.**
167 see Adler, E.
- Fischer, S.**
229 Shahidi, G. G.
- Franaszek, P. A., and R. D. Nelson**
295 *Properties of delay-cost scheduling in time-sharing systems*
- Franchino, A. P.**
201 see Leonovich, G. A.
- Frank, D. J.**
245 see Taur, Y.
- Furman, A.**
51 see Ellis, W. F.
- Gallagher, W. J.**
655 see Kirtley, J. R.
- Gallo, T. A.**
547 see Deutsch, A.
- Geffken, R. M.**
371 see Ryan, J. G.
- Geissler, S. F.**
167 see Adler, E.
- Givens, J. H.**
215 see Koburger, C. W., III
- Gowda, S.**
83 see Shin, H. J.
- Grohoski, G. F.**
5 see Sechler, R. F.
- Gupta, A.**
655 see Kirtley, J. R.
- Gustavson, F. G.**
575 see Agarwal, R. C.
- Hansen, H. H.**
215 see Koburger, C. W., III
- Harper, J. M. E.**
419 see Licata, T. J.
- Hasegawa, Y.**
603 see Avouris, Ph.
- Hedberg, E. L.**
51 see Ellis, W. F.
- Heinzelmann, H.**
669 see McClelland, G. M.
- Heller, L. G.**
33 see Bernstein, K.
- Hoen, S.**
681 see Mamin, H. J.
- Holmes, S. J.**
167 see Adler, E.
- Holmes, S. J.**
189 see Chesebro, D. G.
- Holmes, S. J.**
215 see Koburger, C. W., III
- Horak, D. V.**
215 see Koburger, C. W., III
- Hosokawa, K.**
43 see Sunaga, T.
- Houle, R. M.**
93 see Bechade, R. A.

- Hu, C.-K.,** K. P. Rodbell, T. D. Sullivan, K. Y. Lee, and D. P. Bouldin
465 *Electromigration and stress-induced voiding in fine Al and Al-alloy thin-film lines*
- Jaffe, M. D.**
167 see Adler, E.
- Johnson, J. B.**
167 see Adler, E.
- Joshi, M.**
575 see Agarwal, R. C.
- Kalter, H. L.**
51 see Ellis, W. F.
- Ketchen, M. B.**
655 see Kirtley, J. R.
- Kirihata, T.**
105 see Dhong, S. H.
- Kirtley, J. R.,** M. B. Ketchen, C. C. Tsuei, J. Z. Sun, W. J. Gallagher, Lock See Yu-Jahnes, A. Gupta, K. G. Stawiasz, and S. J. Wind
655 *Design and applications of a scanning SQUID microscope*
- Kitamura, K.**
43 see Sunaga, T.
- Koburger, C. W., III,** W. F. Clark, J. W. Adkisson, E. Adler, P. E. Bakeman, A. S. Bergendahl, A. B. Botula, W. Chang, B. Davari, J. H. Givens, H. H. Hansen, S. J. Holmes, D. V. Horak, C. H. Lam, J. B. Lasky, S. E. Luce, R. W. Mann, G. L. Miles, J. S. Nakos, E. J. Nowak, G. Shahidi, Y. Taur, F. R. White, and M. R. Wordeman
215 *A half-micron CMOS logic generation*
- Koburger, C. W., III**
167 see Adler, E.
- Kopcsay, G. V.**
547 see Deutsch, A.
- Kuchta, D. M.,** H. A. Ainspan, F. J. Canora, and R. P. Schneider, Jr.
63 *Performance of fiber-optic data links using 670-nm cw VCSELs and a monolithic Si photodetector and CMOS preamplifier*
- Kuehlmann, A.,** A. Srinivasan, and D. P. LaPotin
149 *Verity—A formal verification program for custom CMOS circuits*
- Kuehlmann, A.**
131 see Bergamaschi, R. A.
- Lagarias, J. C.,** and C. P. Tresser
283 *A walk along the branches of the extended Farey tree*
- Lam, C. H.**
215 see Koburger, C. W., III
- LaPotin, D. P.**
149 see Kuehlmann, A.
- Lasky, J. B.**
167 see Adler, E.
- Lasky, J. B.**
215 see Koburger, C. W., III
- Lee, H. S.**
51 see Ellis, W. F.
- Lee, K. Y.**
465 see Hu, C.-K.
- Leonovich, G. A.,** A. P. Franchino, W. J. Miller, and U. E. Tsou
201 *Integrated cost and productivity learning in CMOS semiconductor manufacturing*
- Licata, T. J.,** E. G. Colgan, J. M. E. Harper, and S. E. Luce
419 *Interconnect fabrication processes and the development of low-cost wiring for CMOS products*
- Lloyd, B.**
167 see Adler, E.
- Luce, S. E.**
215 see Koburger, C. W., III
- Luce, S. E.**
419 see Licata, T. J.
- Lutz, M. A.,** R. M. Feenstra, and J. O. Chu
629 *Atomic force microscopy studies of SiGe films and Si/SiGe heterostructures*
- Lyo, I.-W.**
603 see Avouris, Ph.
- Maffitt, T. M.**
51 see Ellis, W. F.
- Mallette, R. P.**
189 see Chesebro, D. G.
- Mamin, H. J.,** B. D. Terris, L. S. Fan, S. Hoen, R. C. Barrett, and D. Rugar
681 *High-density data storage using proximal probe techniques*
- Mann, R. W.,** L. A. Clevenger, P. D. Agnello, and F. R. White
403 *Silicides and local interconnections for high-performance VLSI applications*
- Mann, R. W.**
215 see Koburger, C. W., III
- Mate, C. M.**
617 *Force microscopy studies of the molecular origins of friction and lubrication*
- McClelland, G. M.,** H. Heinzelmann, and F. Watanabe
669 *The femtosecond field-emission camera, a device for continuous observation of the motion of individual adsorbed atoms and molecules*
- McFarland, P. A.**
229 see Shahidi, G. G.
- Megdanis, A. C.**
83 see Shin, H. J.
- Mii, Y.-J.**
245 see Taur, Y.
- Mii, Y.-J.**
383 see Edelstein, D. C.
- Miles, G. L.**
167 see Adler, E.
- Miles, G. L.**
215 see Koburger, C. W., III
- Miller, C. P.**
51 see Ellis, W. F.
- Miller, W. J.**
201 see Leonovich, G. A.
- Moricz, M. Z.**
131 see Bergamaschi, R. A.
- Nakos, J. S.**
167 see Adler, E.
- Nakos, J. S.**
215 see Koburger, C. W., III
- Nelson, R. D.**
295 see Franaszek, P. A.
- Nguyen, S. V.**
437 see Cote, D. R.
- Nijjima, H.**
531 *Design of a solid-state file using flash EEPROM*

- Ning, T. H.**
229 see Shahidi, G. G.
- Nobakht, R. A.**
331 *A unified table-based Viterbi subset decoder for high-speed voice-band modems*
- Nobakht, R. A.**
569 *An algorithm for adaptive cancellation of phase jitter*
- Noble, W. P., Jr.**
167 see Adler, E.
- Nowak, E. J.**
33 see Bernstein, K.
- Nowak, E. J.**
189 see Chesebro, D. G.
- Nowak, E. J.**
215 see Koburger, C. W., III
- Nowak, E. J.**
245 see Taur, Y.
- O'Connor, R. A.**
131 see Bergamaschi, R. A.
- Ohta, T.**
523 *Use of multiple representations for simulating cloth shapes and motions: An overview*
- Palkar, P.**
575 see Agarwal, R. C.
- Paraszczak, J. R.**
371 see Ryan, J. G.
- Park, J., S. Vassiliadis, and J. G. Delgado-Frias**
315 *Flexible oblivious router architecture*
- Parker, B. D.**
73 see Ewen, J. F.
- Pearson, D. J.**
83 see Shin, H. J.
- Pennington, S. L.**
437 see Cote, D. R.
- Podlesnik, D. V.**
437 see Cote, D. R.
- Pohl, D. W.**
701 *Some thoughts about scanning probe microscopy, micromechanics, and storage*
- Polcari, M. R.**
229 see Shahidi, G. G.
- Poulin, N. R.**
371 see Ryan, J. G.
- Prakash, S.**
131 see Bergamaschi, R. A.
- Rao, D. S.**
131 see Bergamaschi, R. A.
- Reynolds, S. K.**
83 see Shin, H. J.
- Rishton, S. A.**
245 see Taur, Y.
- Rodbell, K. P.**
465 see Hu, C.-K.
- Rubin, B. J.**
547 see Deutsch, A.
- Rugar, D.**
681 see Mamin, H. J.
- Ryan, J. G., R. M. Geffken, N. R. Poulin, and J. R. Paraszczak**
371 *The evolution of interconnection technology at IBM*
- Sai-Halasaz, G. A.**
245 see Taur, Y.
- Sai-Halasaz, G. A.**
383 see Edelstein, D. C.
- Schneider, R. P., Jr.**
63 see Kuchta, D. M.
- Sechler, R. F., and G. F. Grohoski**
5 *Design at the system level with VLSI CMOS*
- Sechler, R. F.**
23 *Interconnect design with VLSI CMOS*
- Sengle, E. W.**
189 see Chesebro, D. G.
- Shahidi, G. G., J. D. Warnock, J. Comfort, S. Fischer, P. A. McFarland, A. Acovic, T. I. Chappell, B. A. Chappell, T. H. Ning, C. J. Anderson, R. H. Dennard, J. Y.-C. Sun, M. R. Polcari, and B. Davari**
229 *CMOS scaling in the 0.1- μ m, 1.X-volt regime for high-performance applications*
- Shahidi, G.**
215 see Koburger, C. W., III
- Shin, H. J., D. J. Pearson, S. K. Reynolds, A. C. Megdanis, S. Gowda, and K. R. Wrenner**
83 *Custom design of CMOS low-power high-performance digital signal-processing macro for hard-disk-drive applications*
- Soyuer, M.**
73 see Ewen, J. F.
- Srinivasan, A.**
149 see Kuehlmann, A.
- Stamper, A. K.**
437 see Cote, D. R.
- Stapper, C. H.**
51 see Ellis, W. F.
- Stawiasz, K. G.**
655 see Kirtley, J. R.
- Stok, L.**
131 see Bergamaschi, R. A.
- Sullivan, T. D.**
465 see Hu, C.-K.
- Sun, J. Y.-C.**
229 see Shahidi, G. G.
- Sun, J. Z.**
655 see Kirtley, J. R.
- Sunaga, T., K. Hosokawa, S. H. Dhong, and K. Kitamura**
43 *A 64Kb $\times$ 32 DRAM for graphics applications*
- Surovic, C. W.**
547 see Deutsch, A.
- Surya, S.**
113 see Bose, P.
- Tanaka, M.**
105 see Dhong, S. H.
- Taur, Y., Y.-J. Mii, D. J. Frank, H.-S. Wong, D. A. Buchanan, S. J. Wind, S. A. Rishton, G. A. Sai-Halasaz, and E. J. Nowak**
245 *CMOS scaling into the 21st century: 0.1 μ m and beyond*
- Taur, Y.**
215 see Koburger, C. W., III
- Terman, L. M.**
547 see Deutsch, A.
- Terris, B. D.**
681 see Mamin, H. J.
- Tomashot, S. W.**
105 see Dhong, S. H.

Tresser, C. P.
 283 see Lagarias, J. C.
Tsou, U. E.
 201 see Leonovich, G. A.
Tsuei, C. C.
 655 see Kirtley, J. R.
Vassiliadis, S.
 315 see Park, J.
Voldman, S. H.
 167 see Adler, E.
Voldman, S. H.
 189 see Chesebro, D. G.
Warnock, J. D.
 229 see Shahidi, G. G.
Watanabe, F.
 669 see McClelland, G. M.
Weeks, T. W.
 189 see Chesebro, D. G.
White, F. R.
 33 see Bernstein, K.
White, F. R.
 215 see Koburger, C. W., III
White, F. R.
 403 see Mann, R. W.
Widmer, A. X.
 73 see Ewen, J. F.
Wilson, R. J.
 639 see Chambliss, D. D.
Wind, S. J.
 245 see Taur, Y.
Wind, S. J.
 655 see Kirtley, J. R.
Wong, H.-S.
 245 see Taur, Y.
Wordeman, M. R.
 215 see Koburger, C. W., III
Wrenner, K. R.
 73 see Ewen, J. F.
Wrenner, K. R.
 83 see Shin, H. J.
Yu-Jahnes, Lock See
 655 see Kirtley, J. R.